In the Claims:

The claims are as follows:

1. (Original) An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad; and

a solder member electrically coupling the first pad to the second pad.

2. (Original) The electronic structure of claim 1, wherein a coefficient of thermal expansion (CTE) of the organic substrate is between about 10 ppm/°C and about 18 ppm/°C.

3. (Original) The electronic structure of claim 1, wherein P is between about .15 and about .75, wherein P is defined as $(C_{SOLDER} - C_{ORGANIC})/(C_{SOLDER} - C_{SEMI})$, wherein C_{SOLDER} is a CTE of the solder member, wherein $C_{ORGANIC}$ is a CTE of the organic substrate, and wherein C_{SEMI} is a CTE of the semiconductor substrate.

4. (Original) The electronic structure of claim 1, wherein the organic substrate includes an organic material selected from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene, and combinations thereof.

5. (Original) The electronic structure of claim 1, wherein the solder member includes a controlled collapse chip connection (C4) solder ball.

6. (Original) The electronic structure of claim 1, wherein the solder member includes a lead-tin alloy.

7. (Original) An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad;

a solder member electrically coupling the first pad to the second pad; and

an underfill material between the semiconductor substrate and the organic substrate, wherein the underfill material encapsulates the solder member, and wherein the underfill material has an elastic modulus of at least about 1 gigapascal.

8. (Original) An electronic structure, comprising:

a semiconductor chip having a first electrically conductive pad thereon;

an organic chip carrier having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad;

a solder member electrically coupling the first pad to the second pad; and

an underfill material between the semiconductor chip and the organic chip carrier, wherein the underfill material encapsulates the solder member, and wherein the underfill material has an elastic modulus of at least about 1 gigapascal.

9. (Original) An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad by a factor of at least about 1.2; and

a solder member electrically coupling the first pad to the second pad.

10. (Original) An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad by a factor between about 1.1 and about 1.3; and

a solder member electrically coupling the first pad to the second pad.

11. (Original) An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad by a factor between about 1.3 and about 2.0; and

a solder member electrically coupling the first pad to the second pad.

12. (Original) An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon; and

a solder member electrically coupling the first pad to the second pad, wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.25 mm.

13. (Original) The electronic structure of claim 12, wherein a coefficient of thermal expansion (CTE) of the organic substrate is between about 10 ppm/°C and about 18 ppm/°C.

14. (Original) The electronic structure of claim 12, wherein P is between about .15 and about .75, wherein P is defined as $(C_{SOLDER} - C_{ORGANIC})/(C_{SOLDER} - C_{SEMI})$, wherein C_{SOLDER} is a CTE of the solder member, wherein $C_{ORGANIC}$ is a CTE of the organic substrate, and wherein C_{SEMI} is a CTE of the semiconductor substrate.

15. (Original) The electronic structure of claim 12, wherein the organic substrate includes an organic material selected from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene, and combinations thereof.

16. (Original) The electronic structure of claim 12, wherein the solder member includes a controlled collapse chip connection (C4) solder ball.

17. (Original) The electronic structure of claim 12, wherein the solder member includes a lead-tin

alloy.

18. (Original) An electronic structure, comprising:

a semiconductor chip having a first electrically conductive pad thereon;

an organic chip carrier having a second electrically conductive pad thereon;

a solder member electrically coupling the first pad to the second pad, wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.25 mm; and

an underfill material between the semiconductor chip and the organic chip carrier, wherein the underfill material encapsulates the solder member, and wherein the underfill material has an elastic modulus of at least about 1 gigapascal.

20. (Original) An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon; and

a solder member electrically coupling the first pad to the second pad, wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.40 mm.

Claims 21-40 (withdrawn).